## REMARKS

The above Amendments and these Remarks are in reply to the Office Action mailed December 20, 2005.

Currently, claims 1-36 are pending. Applicants respectfully request reconsideration of claims 1-36.

I. Summary of the Examiner's Objections

Claims 1-3, 5-17, 19, 20 and 25-36 were rejected under 35 USC 102(e) as being anticipated by *Lee* (USP 6,795,366).

Claims 4 and 18 were rejected under 35 USC 103(a) as being unpatentable over *Lee* (USP 6,795,366) in view of *Hellums* (5,362,988) (previously cited).

Claims 21-24 were rejected under 35 U.S.C. 103(a) as being unpatentable over *Lee* (USP 6,795,366).

II. Summary of the Amendments

Applicant has amended claims 1, 25, 32, and 34 herein.

III. Remarks

It is respectfully submitted Claims 1-3, 5-17, 19, 20 and 25-36 are not anticipated under 35 U.S.C. § 102(e) as anticipated by Lee (United States Patent 6,795,366).

Lee does not disclose: "a bypass enable signal output by the controller subsequent to the power of complete signal being generated by the host device indicating that the power of the host is complete". In addition, the Lee reference does not disclose "... the host device supplying ... a power up *during* complete a signal". Rather, to the extent Lee discloses any bypass, it discloses the bypass is enabled power up (not after it), and disabled when a threshold is exceeded.

The circuits shown in Figures 7, 14 and 16 of Lee, cited by the Examiner as providing the

aforementioned limitations, actually clearly disclose the opposite. Turning first to Figure 7, it is respectfully submitted that the circuit 120 shown in Figure 7 (cited as generating a power up complete signal) is not part of the "host device". In fact, the specification is clear that the power level detector 120 actually constitutes a part of the memory system:

> The memory device comprises an internal circuit 60, an Internal Voltage Controller (IVC) 500, a standby IVC driver 200, a power level detector 120, a CE buffer 140, and a CMD buffer 160. (Specification, Column 1, Line 36-39).

Hence, Lee does not disclose a "host device supplying a … power up a complete signal".

In addition, Lee does not disclose a "bypass enable signal" as described. With reference to Figure 14, it is respectfully submitted that the Examiner's interpretation of the Lee reference is in fact opposite of what the reference teaches: the reference shows that the bypass is ***enabled*** during power up of the device, and ***disabled*** when Vext exceeds a specific level:

> As may be seen from FIG. 16, the power-up PowerUp (PDT) inputs to an inverter INV2 to turn on p-mos transistor MP4, effectively shorting Vext to Vint. (*During the power- up period, the power-up signal PowerUp (PDT) goes to a logic HIGH. The gate of the p-mos transistor goes to logic LOW via an inverter INV2. The p-mos transistor MP4 turns on and the external supply voltage Vext is connected to the internal supply voltage Vint via the on transistor, effectively shorting Vext to Vint.)*
>
> … During the power up, the internal supply voltage Vint ramps up and precisely tracks the external supply voltage Vext until time t1. At that time, the internal supply voltage reaches the minimum operating voltage Vdet. After the power-up signal PDT goes to a logic LOW, as described above in connection with the first embodiment of invention, the slope of the internal supply voltage Vint tracks that of the standby IVC driver …" (Specification Column 5, Lines 56 – Column 6, Line 10. (Emphasis added))

Hence, Lee does not provide a "bypass enable signal". Lee provides a "bypass disable signal" which is not generated by a host device.

Hence, it is respectfully submitted that Claim 1 is not anticipated by Lee. It is further respectfully submitted that claims 2 – 3, 5 – 15 are likewise not anticipated by Lee as each of said claims is dependent

on claim 1 and includes all the limitations of claim 1.

With respect to Independent Claim 16, and in view of the foregoing discussion, it is respectfully submitted that Lee does not disclose the step of "setting the bypass to off prior to power up of a host device" nor the steps of

> "responsive to a power up completion signal from a host device to the controller, determining the power supplied by the host; and
> if the power is below a threshold operating voltage, enabling the bypass using the controller."

Lee never discloses "setting the bypass to off prior to power up of a host device". Lee discloses setting the bypass to "on". With respect to the step of setting, the Examiner states "Figure 17 shows the transistor MP4 is off until Vint goes vertical". In fact, Figure 17 shows the ramping of the internal and external voltages being identical (bypass enabled) prior to power up completion. Contrary to the examiner's assertion, the bypass is "on" prior to power up of the host device, in direct contradiction to the limitations of the current claims. Moreover, there is no step of "enabling the bypass using the controller … if the power is below a threshold operating voltage". In the Lee reference, the bypass is always enabled, and disabled once the external voltage exceeds the threshold level.

Hence, for the reasons set forth above, it is respectfully submitted that Claims 16, and claims 17, 19, 20 dependent there from and including all the limitations of claim 16 are not anticipated by Lee.

Further with respect to Independent Claim 25, it is respectfully submitted that Lee does not disclose a "peripheral device including … a controller" nor "a bypass control signal output from the controller coupled to the bypass element and responsive to a host system power up completed signal *which enables the bypass element when the host voltage is below a threshold level subsequent to host power-up completion".* As noted above, the bypass element is enabled constantly before any power up completed signal reaches the bypass circuit. Moreover, the power up completed signal in the Lee

reference is not provided by a host system.

For the reasons set forth above with respect to Claims 1 and 16, it is respectfully submitted that Claims 25-31 are not anticipated under 35 U.S.C. § 102(e) by Lee.

Further with respect to claim 32, it is respectfully submitted that Lee fails to disclose:

> setting the bypass to off prior to power up of a host device;
> responsive to a command signal from the host device, determining the power supplied by the host; and
> if the power is below a threshold operating voltage subsequent to host power-up completion, enabling the bypass using the controller

The limitations of claim 32 are similar to those set forth above with respect to claim 16 and for the reasons set forth above with respect to claim 16, it is submitted claim 32 and claim 33 dependent therefrom is not anticipated by Lee.

Further with respect to Claim 34, it is respectfully submitted that there is no disclosure of:

> ... voltage regulator having a shorting element between a host voltage input and an output, the shorting element being responsive to the bypass control signal, the bypass control signal provided by the controller responsive to a host system power up complete signal which enables a shorting element when the host supply voltage provided by the host is below a threshold level subsequent to power up completion.

As noted above, when any power up complete signal is provided by a circuit 120, prior to that time, the bypass is enabled. The power up complete signal disables the bypass.

For the reasons set forth above with respect to Claims 1, 16 and 25 it is respectfully submitted that Claim 34 and claims 35 and 36 dependent there from are not anticipated.

It is further respectfully submitted that Claims 4 and 18, 21-24 are not obvious in view of Lee alone or taken with Hellums (United States Patent 5,362,988). Lee maintains the bypass as enabled when the threshold voltage is below a particular level. When a power up completed signal is received, Lee disables the bypass. Hence, Lee acts in direct contradiction to the claimed invention. No combination of

Lee with Hellums avoids the direct teaching away of the claimed invention by Lee. Lee teaches that one enables the bypass to achieve the advantage of providing "a quickly ramped-up internal supply voltage… within the system required time". In contrast, the advantage of the present invention is that over-voltage protection is achieved by not enabling the bypass until a power up complete signal is received and the supply voltage is below a threshold.

Hence, it is respectfully submitted that claims 4 and 18, 21-24 are not obvious in view of Lee alone or taken with Hellums.

For the reasons set forth above, it is respectfully submitted that all Claims set forth herein are therefore allowable.

Based on the above amendments and these remarks, reconsideration of claims 1-36 is respectfully requested.

Request for Initialed Information Disclosure Statements

It is noted that the Information Disclosures submitted July 20, 2004 and September 12, 2005 have not been returned as initialed and signed, indicating consideration by the Examiner. While the USPTO's Transaction History shows such Disclosures were considered, initialed copies of such Disclosures are respectfully requested.

* * *

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

Enclosed is a PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.136 for extending the time to respond up to and including today, June 20, 2006.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for

extension of time, which may be required.

Respectfully submitted,

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